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Engineering Note

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Project: CFT Axial Front End
Doc. No: A990108a

Subject: SPICE simulations of charge split networks & SIFT Preamp

Introduction

This document provides a summary analysis of charge splitting networks for the CFT boards, looking at how well the networks will function and dependence upon component tolerance.

The CFT Axial Circuit

The fiber tracking boards have a simple circuit in which all the charge produced by the VLPC goes into the SIFT. Figure 1 shows a schematic representation of this circuit in a generic form. The SIFT preamp model is the same as that used previously by Dave Huffman to analyze the input impedance of the SIFT. Numerous control parameters are available to the circuit designer:

- Cs is the series capacitance which DC isolates the input of the SIFT preamp from the VLPC.
- Cc is the inherent capacitance of the Flex Cable, which does bleed off some of the charge generated by the VLPC.
- Cd is an optional drain capacitance which forms a charge splitting network with Cs.
- Rd is a drain resistor used to complete the DC bias path for the VLPC.
- RCable models the series resistance of the flex cable.
- Vphdr is a control voltage used by the SIFT to 'preset' the preamplifier output voltage.

In this first simulation the effects of the various passive components are examined with the VLPC replaced by a simple resistor. No charge signals are being measured here; we first look at the reasonable bounds of the controllable parameters.

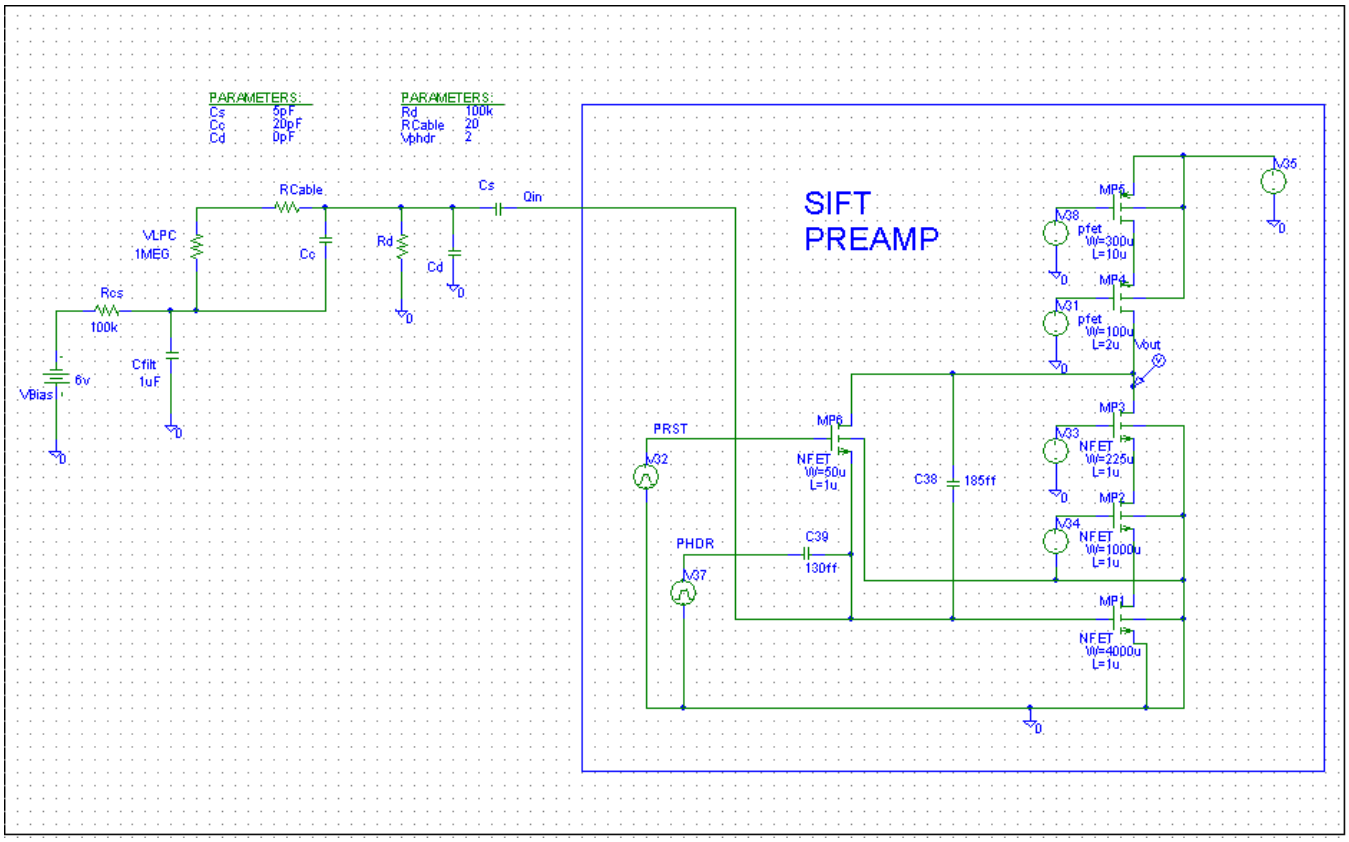

Figure 1

Previous engineering notes (see http://d0server1/users/janderson/Public~1/a981218a.pdf) indicate that various time constants associated with the R's and C's may be critical. The circuit shown in Figure 1 should put all the charge into the SIFT and virtually none should be shunted, as Cs is much larger than Cc and Cd has been set to zero. However, the engineering note suggests that this large value of Cs may cause trouble. A simulation run for various values of Cs (10pf – 10000pF, 3 pts/decade) is given as Figure 2. The figure shows the resulting output voltage Vout, which is presented to the discriminator inside the SIFT, along with the current which flows in the series capacitor Cs.

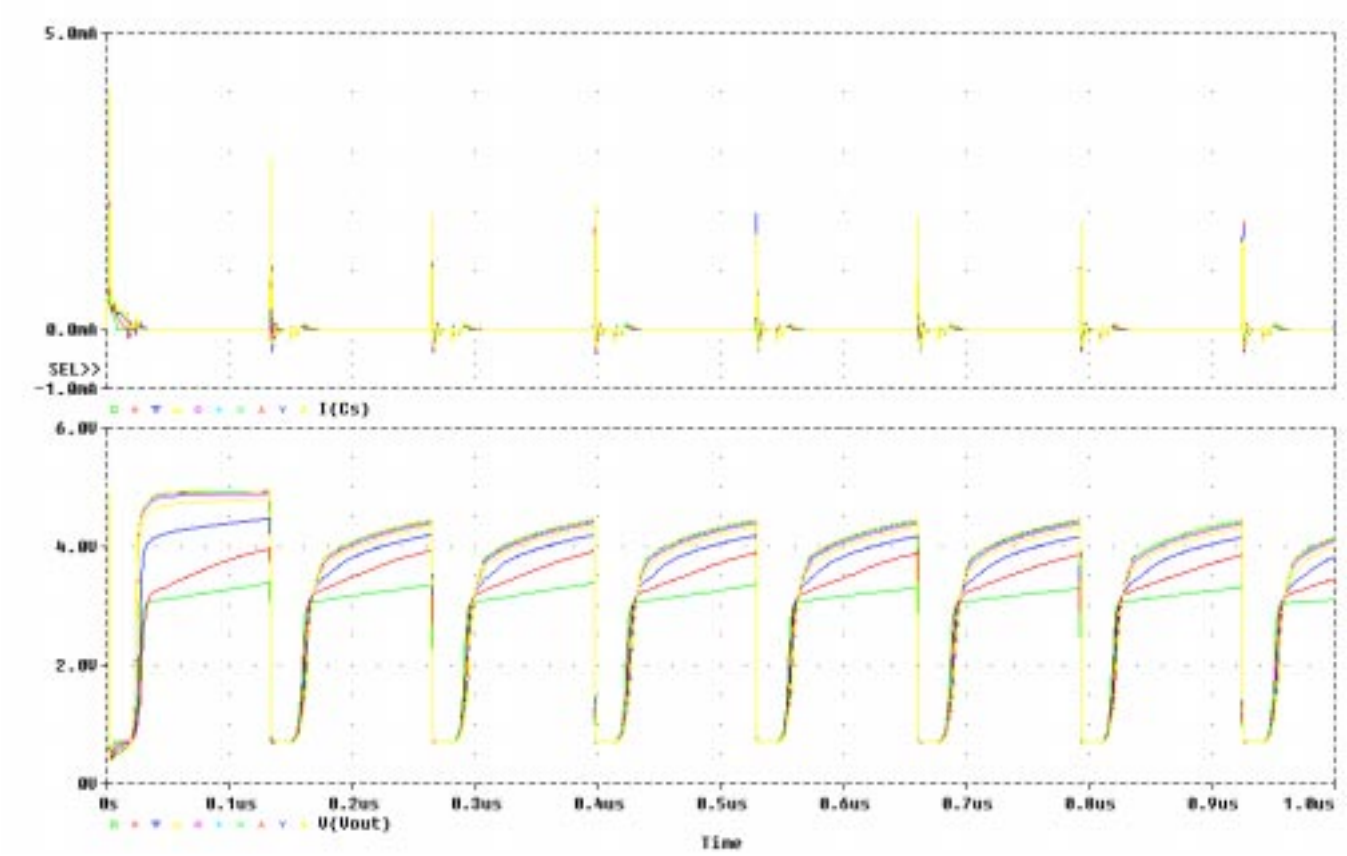

Figure 2

As Cs increases, not only does the baseline of the SIFT output voltage change, so also does the slope during the acquisition interval. The current plot shows that there are some very large and unbalanced currents which flow in Cs during the reset interval. If these currents are real, then the SIFT can't possibly work as charge would accumulate on the input side every cycle. This is known not to be true, so the SPICE model of the SIFT may have some serious difficulties. Even if Cs is reduced to 5 pF and Cd increased to 50 pF, the net charge acquired from the reset is on the order of 16 fC per cycle. This indicates that the matching of the transistors in the model is nowhere near good enough to estimate analog performance.

A simpler model of the SIFT input which may suffice for charge splitting calculations is that of a simple resistor in series with a capacitor. At low frequencies (~20 MHz) the SIFT appears to have an input impedance of about 600 ohms. At higher frequencies (~150 MHz) the impedance drops to about 200 ohms. So, a model of a 200 ohm resistor in series with a 20 pF capacitor is reasonably close. This new circuit is shown in Figure 3.

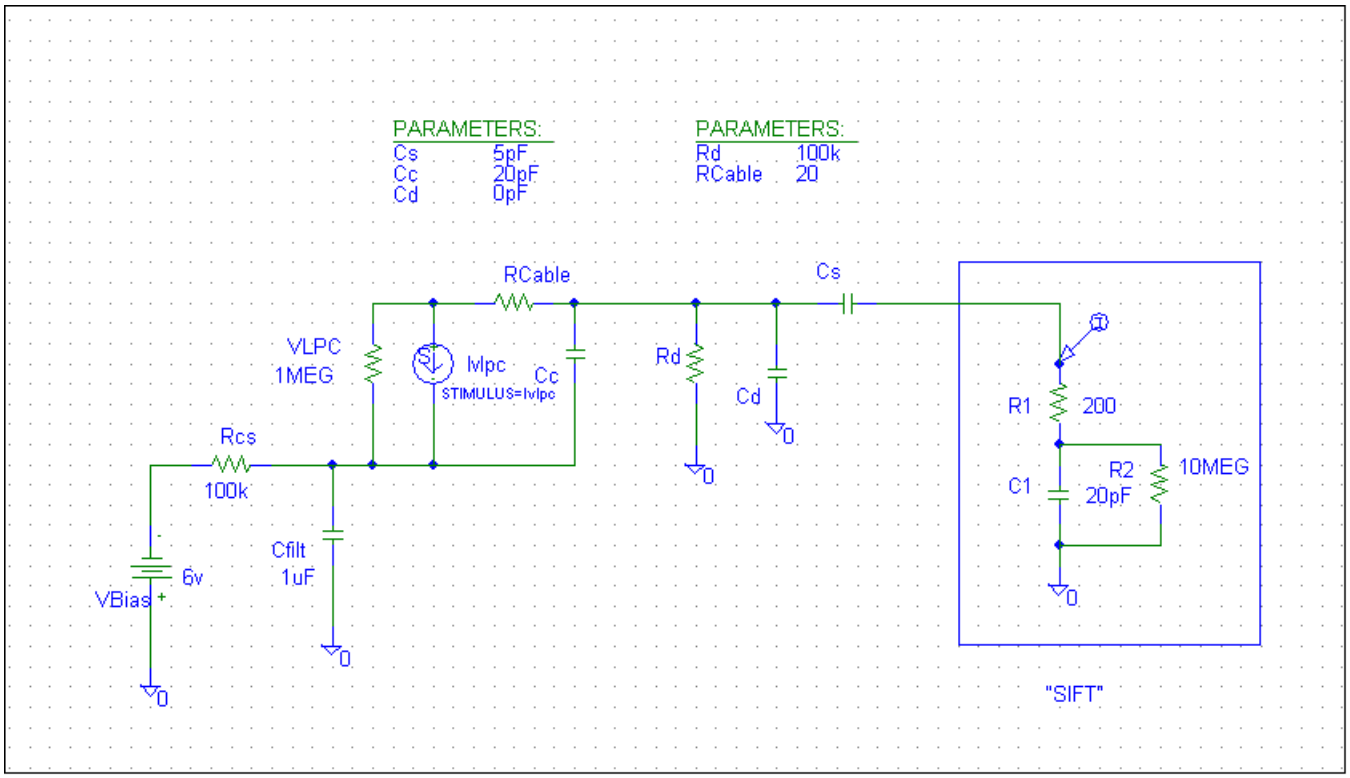

Figure 3

Ivlpc is a model of the VLPC current, which is set to deliver 15fCoul of charge at time T=40ns. The VLPC resistor is present to model the dark current of the VLPC. The integral of the current entering R1 (inside the "SIFT") shows the charge as measured for three decades of Cs, from 10pF to 10000pF; this is given in Figure 4. Since Cc is the only other path for the charge to go (Cd is set to zero), whatever doesn't go through Cs and R1 goes through Cc.

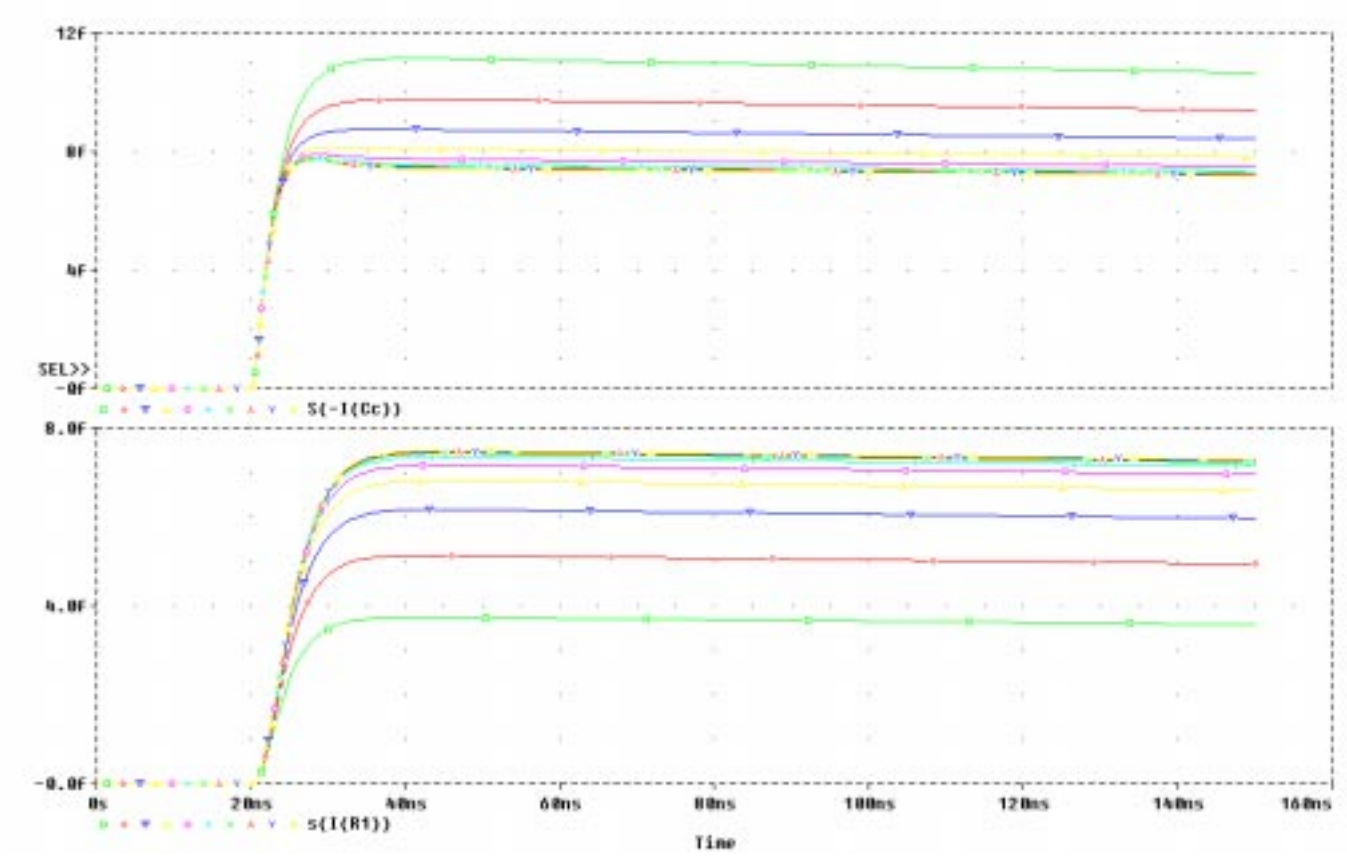

Figure 4

Note that the integral shows a visible relaxation (negative slope) during the remainder of the 132 nsec crossing interval; this is due to losses through Rd. If Rd is increased a bit, to 470K, things get better as shown in Figure 5.

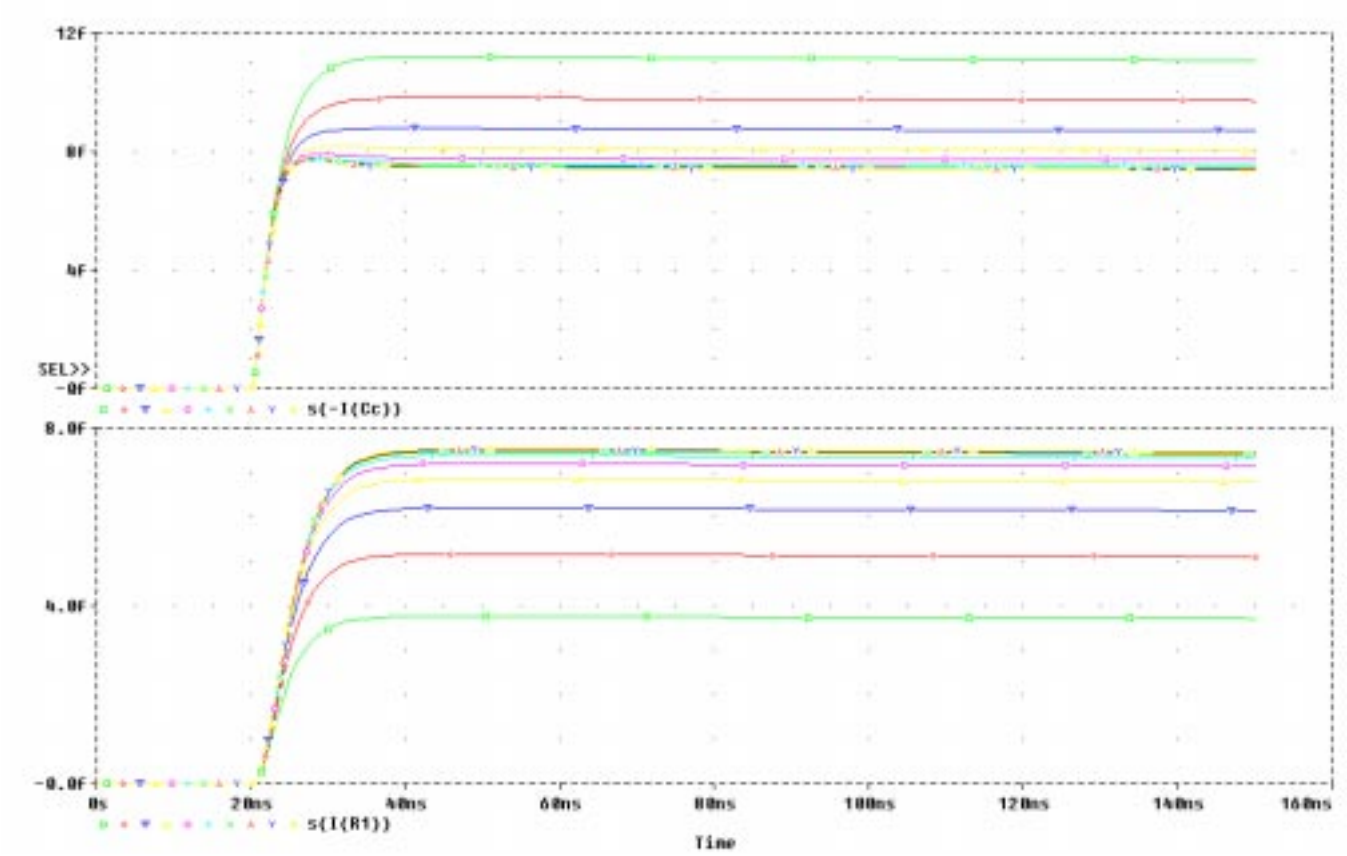

Figure 5

Comparison to the FPS(Front) input with Split Charge

By way of comparison, a variation of the circuit with two SIFT models is shown in Figure 6. This scenario models the Forward Preshower boards, where the input charge is connected to two SIFTs for dual threshold measurements. Based upon the most recent E-mails, the two Cs values are fixed at 25 pF and 117 pF, which should result in a gain ratio of 25/117 or about 0.21. No Cd is used and Cc stays at the estimated cable capacitance of 20 pF.

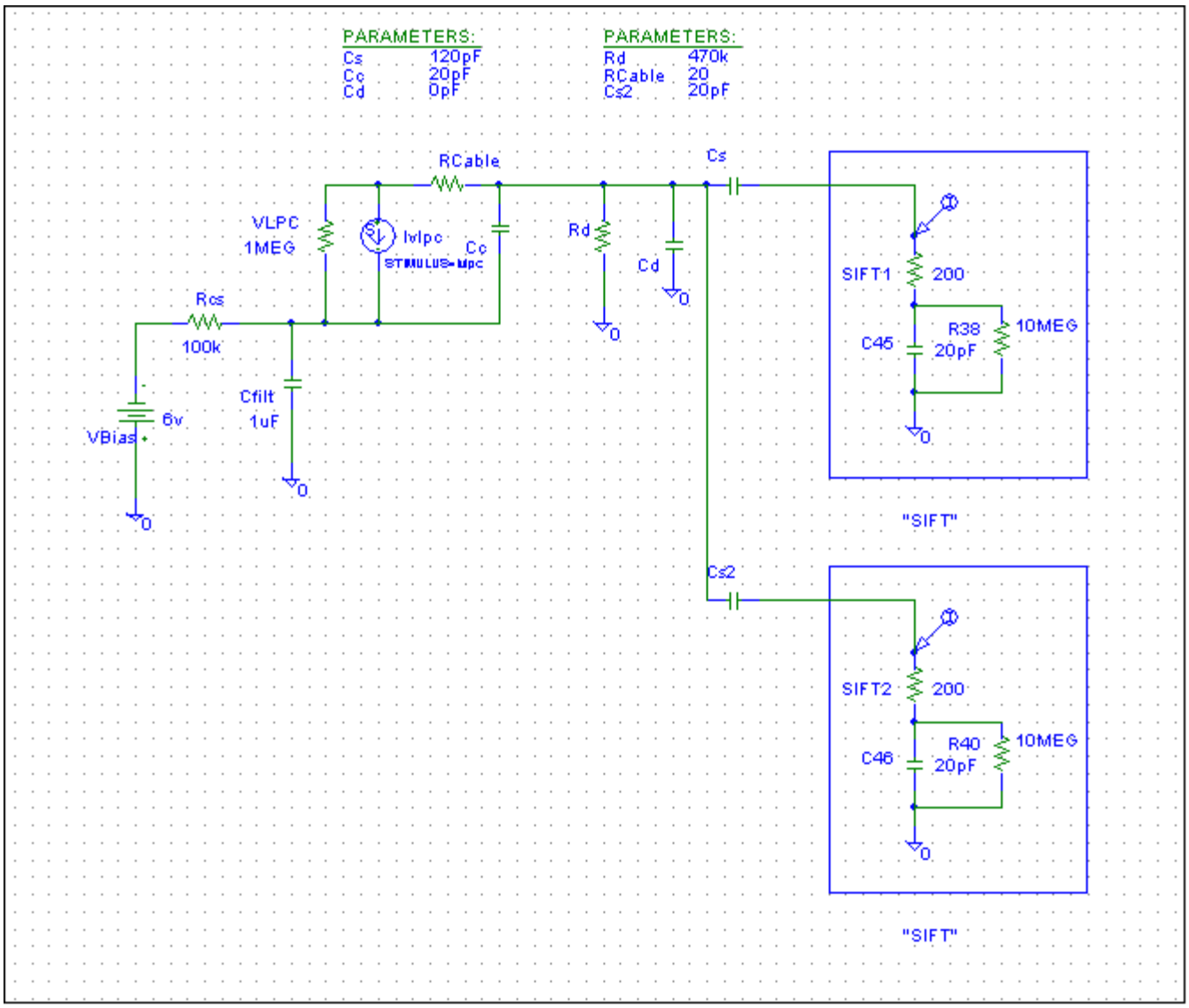

Figure 6

A transient analysis shows that the charge does split, but not as expected. The SIFT with the 120 pF capacitor sees about 35% of the total charge, and the other sees about 22% of the total charge, for a ratio of 0.62, not the 0.21 desired.

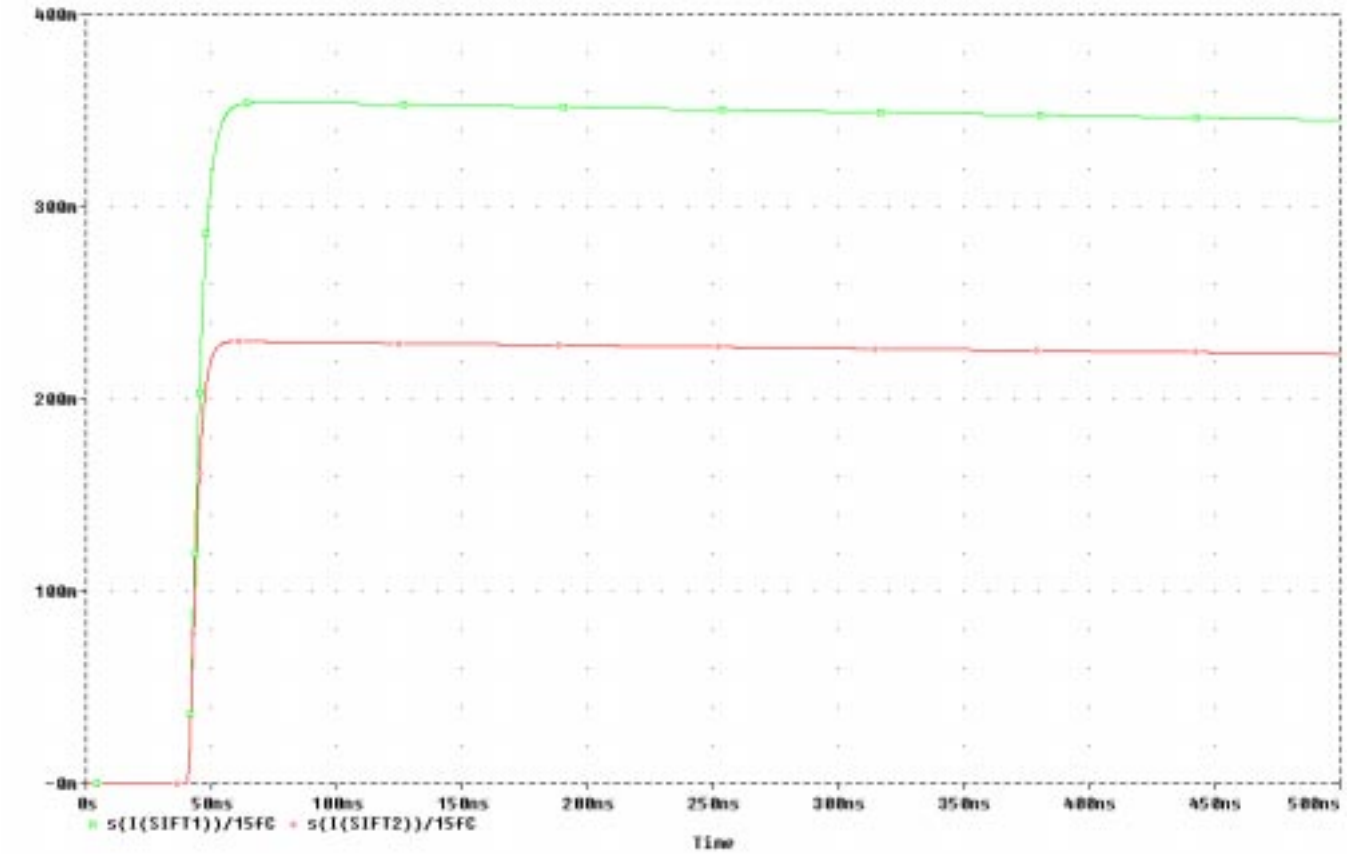

Figure 7

If the Cs capacitances are made smaller, better results can be achieved. Figure 8 shows the ratio of charge delivered to the two SIFTs as a function of Cs2 (1pF to 100pF), with Cs fixed at 20pF.

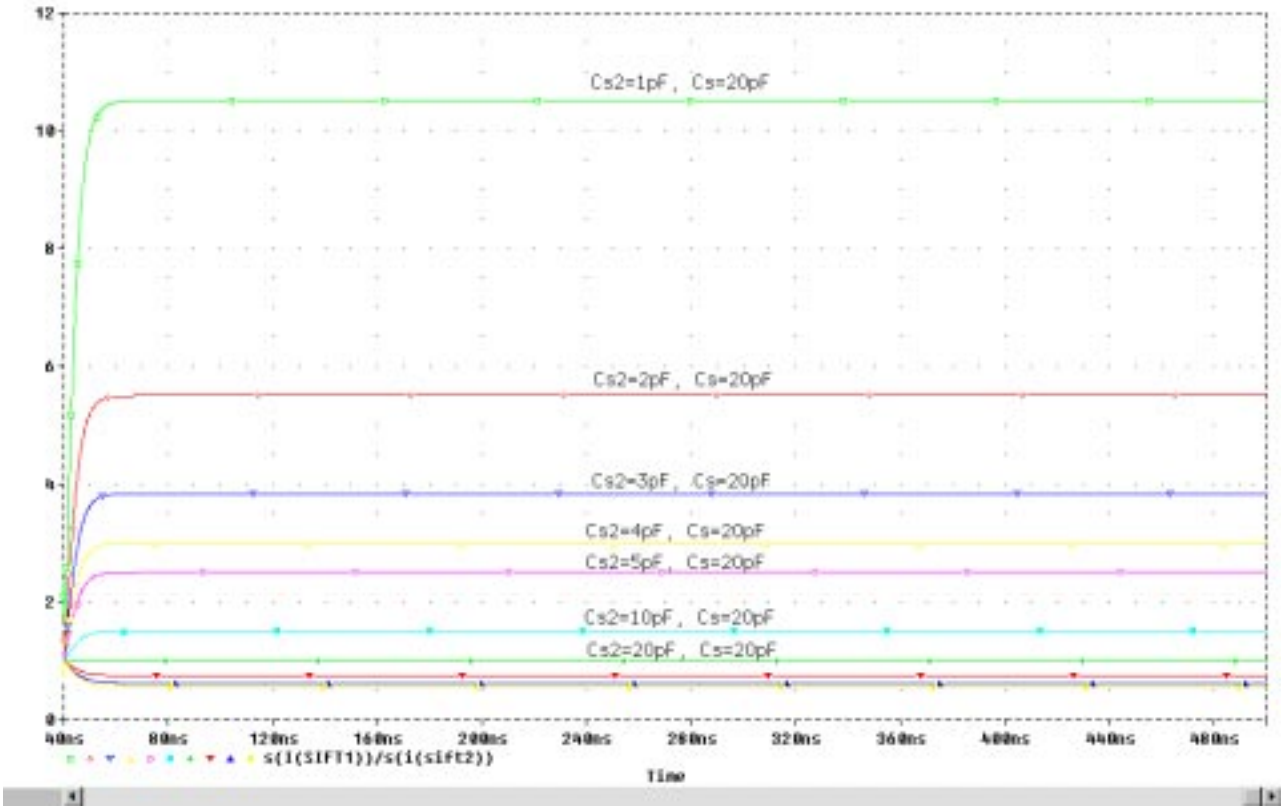

Figure 8

The charge division ratio does vary with the Cs value, and the division ratios work better for smaller capacitors. The values in Figure 8 are summarized in Table 1.

Cs	Cs2	Expected division ratio	Actual division ratio
20pF	1pF	20:1	10.52:1
20pF	2pF	10:1	5.50:1
20pF	3pF	6.67:1	3.83:1
20pF	4pF	5:1	3.00:1
20pF	5pF	4:1	2.50:1
20pF	10pF	2:1	1.50:1
20pF	20pF	1:1	1:1
20pF	40pF	1:2	1:1.33
20pF	80pF	1:4	1:1.61
20pF	160pF	1:8	1:1.79

Table 1

The large deviation from the expected ratio seen for large capacitances can be explained by the relative ratio of Cc to Cs or Cs2. The ideal current source I_{VLPC} is connected to the charge splitter by combination of Rcable and Cc. So long as the impedance of Cs and/or Cs2 is large with respect to the impedance of Cc in parallel with Rd, the charge division is fairly accurate. However, when the impedance of Cs or Cs2 gets smaller, the current shunted by Cc increases and the ratios move. For division ratios away from unity to be reasonably accurate, the impedance of Cs in parallel with the impedance of Cs2 should be no less than a fraction of the impedance of the impedance of Cc in parallel with Rd and Cd. For example, if Cs is 2pF and Cs2 were 100fF (factor of 10 change, but ratio still 20:1), the division ratio improves from 10.52:1 to 18.27:1. Of course, such improvement is possible only within the simulation; 100 fF capacitors are not a practical discrete component value.

Forward Preshower (Back) Charge Splits

Current estimates give the charge splitting in the FPS (back) as 13% of the charge into one SIFT, 4.5% of the charge into the other, and 82.5% drained through Cd and/or Cc. Based on straight division, the values of Cs and Cs2 would then be 11.8pF and 4.1 pF. However, the same charge splitting error as seen previously will also occur here, and so the simulator is used to determine the correct value of Cs to get the right ratios. Figure 9 shows the percentage of charge through each leg as Cs is varied from 1pF to 100pF.

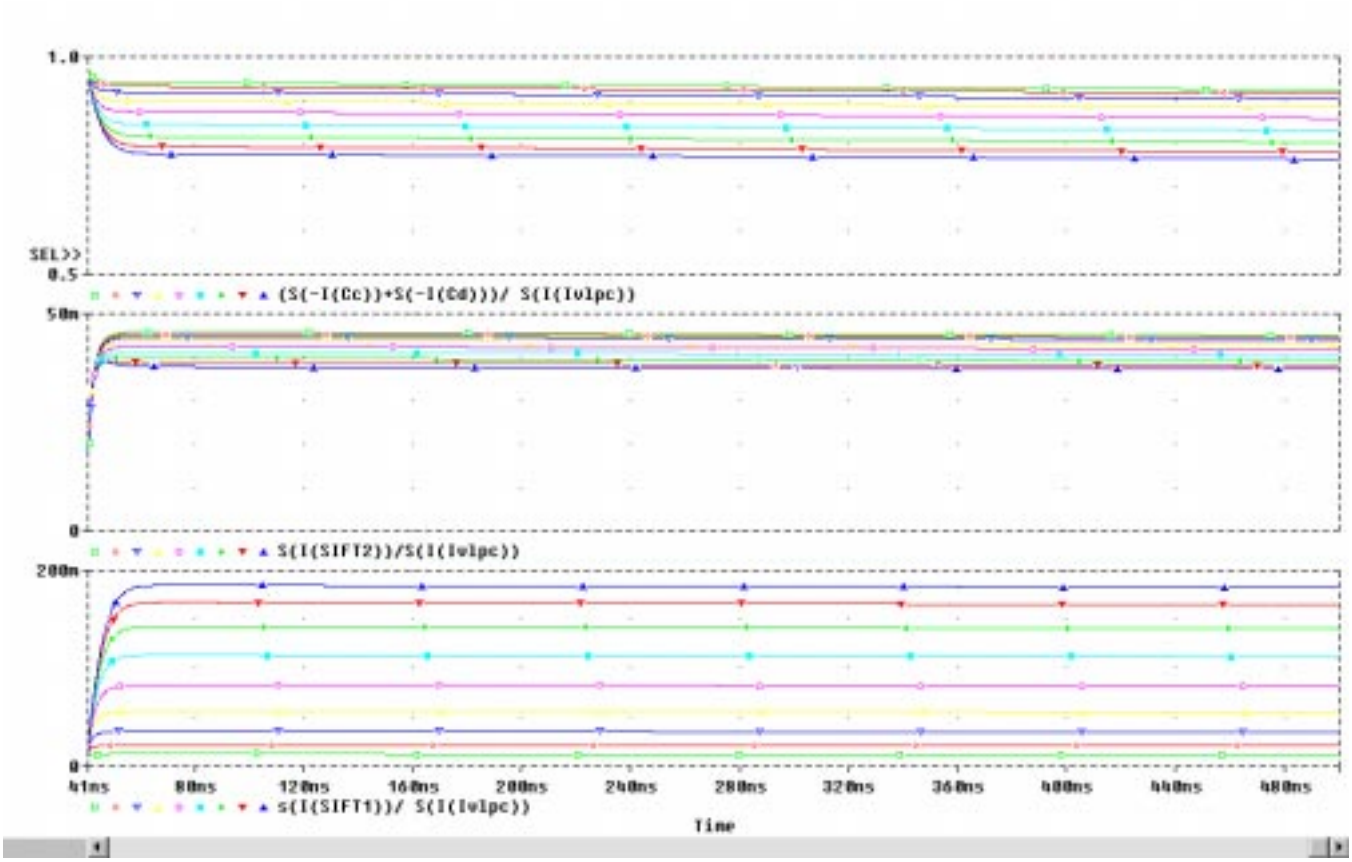

Figure 9

Examination with the Probe cursor function shows that for Cs = 33 pF, the desired charge split is obtained. This is in keeping with Table 1 above, where for a 3:1 actual split a capacitor ratio of 5:1 is required. The error here is even larger than the table's value because the FPS back uses a Cd, making the drain impedance that much lower.